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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS
Patent Owner

Case IPR2013-00006
Patent 6,888,204 B1

Before SALLY GARDNER LANE, BRYAN F. MOORE, and MICHAEL J. FITZPATRICK, *Administrative Patent Judges.*

FITZPATRICK, *Administrative Patent Judge.*

DECISION TO INSTITUTE
TRIAL FOR INTER PARTES REVIEW

BACKGROUND

Micron Technology, Inc. ("Micron") filed a Petition[1] requesting inter partes review of all claims (i.e., claims 1-18) of U.S. Patent 6,888,204 B1 (the "'204 Patent") pursuant to 35 U.S.C. § 311. The Patent Owner, the Board of Trustees of the University of Illinois ("University"), filed a Preliminary Response[2] pursuant to 35 U.S.C. § 313. We have jurisdiction under 35 U.S.C. § 314.

Institution of inter partes review is authorized by statute when "the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. §314(a); *see also* 37 C.F.R. § 42.108.

We determine that the petition demonstrates that there is a reasonable likelihood that Micron would prevail with respect to at least one challenged claim, and we institute inter partes review as to claims 1-18 of the '204 Patent.

A. Related Proceedings

Micron indicates that it is a named defendant in pending litigation concerning the '204 Patent brought by the Patent Owner and styled *The Board of Trustees of the University of Illinois v. Micron Technology, Inc.*, Case No. 2:11-cv-02288 (C.D. Ill.). (Pet. 1.)

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[1] Citations to the Petition may be abbreviated as "Pet."
[2] Citations to the Preliminary Response may be abbreviated as "Prelim. Resp."

Micron also has filed two additional petitions for inter partes review of two related patents: IPR2013-00005 regarding U.S. Patent 6,444,533 and IPR2013-00008 regarding U.S. Patent 5,872,387.

B. The '204 Patent

The '204 Patent (Ex. 1002), entitled "Semiconductor Devices And Methods For Same," issued on May 3, 2005, names Joseph W. Lyding and Karl Hess as inventors, and is assigned to the University. The '204 Patent issued from U.S. Application Serial No. 09/160,657, filed September 25, 1998.

The '204 Patent "relates to methods for treating semiconductor devices or components thereof in order to reduce the degradation of semiconductor device characteristics over time." (Col. 1, ll. 22-25.) In particular, the '204 Patent discloses methods of treating a semiconductor device by passivating (or annealing) the device with deuterium, an isotope of hydrogen. (Col. 2, ll. 36-39; Prelim. Resp. 1.) The '204 Patent explains:

> [T]reatment with deuterium provides a reduction in the depassivation or "aging" of semiconductor devices due to hot-carrier effects. Such aging is evidenced, for example, by substantial degradations of threshold voltage, transconductance, or other device characteristics. In accordance with the present invention, semiconductor devices are fabricated using deuterium to condition the devices and stably reduce the extent of these degradations. (Col. 3, ll. 40-48.)

Prior to the '204 Patent, passivating with hydrogen[3] was "a well-known and established practice in the fabrication of semiconductor devices"

[3] Our use of the term "hydrogen" and the symbol "H" in this Decision refers to naturally occurring hydrogen, which we understand to be predominantly protium but may include trace amounts of deuterium.

to remove defects that affect the operation of the devices. ('204 Patent col. 1, ll. 26-28; U.S. Patent 5,872,387 col. 1, ll. 10-14[4]; *see also* Reed Decl. ¶¶ 13-14.) According to the '204 Patent, it was "discovered that semiconductor devices, for example including MOS[5] devices, can be advantageously treated with deuterium to improve their operational characteristics." (Col. 2, ll. 32-36.)

C. Illustrative Claim

Independent claim 6 is representative of the claimed subject matter and read as follows:

> 6. A semiconductor device comprising an n-channel field effect transistor having an interface between a semiconductive silicon layer and a gate insulating layer having a thickness not exceeding about 55 Angstroms, a drain formed in said semiconductive silicon layer, a source formed in said semiconductive silicon layer, a channel extending between the drain and the source, said gate insulating layer over said channel, said interface between said gate insulating layer and said channel, and conductive contacts for said drain, said source and said gate insulating layer; said semiconductive device structurally characterized by post-fabrication heating of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200 C. to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

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[4] U.S. Patent 5,872,387 issued from U.S. Application Serial No. 08/586,411, filed January 16, 1996, which is the earliest application to which the '204 Patent claims priority. It is not an exhibit in the instant proceeding although it is the subject of another Micron petition, case number IPR2013-00008.

[5] MOS refers to metal oxide semiconductor. ('204 Patent col. 1, ll. 44-45; Reed Decl. ¶ 9.)

D. Prior Art Relied Upon

Micron challenges the patentability of claims 1-18 in view of the following items of prior art:

Ex. 1004	WO 94/19829 to Lisenker et al., published September 1, 1994 ("Lisenker")
Ex. 1005	Mikawa et al., "Electron Spin Resonance Study of Interface States Induced by Electron Injection in Metal-Oxide-Semiconductor Devices," 59 (6) J. Appl. Phys, 2054, March 15, 1986 ("Mikawa")
Ex. 1007	US 5,478,765 to Kwong et al., issued December 26, 1995 ("Kwong")
Ex. 1008	US 4,980,307 to Ito et al., issued December 25, 1990 ("Ito")
Ex. 1009	US 4,027,380 to Deal et al., issued June 7, 1977 ("Deal")
Ex. 1010	Gise et al., "Semiconductor and Integrated Circuit Fabrication Techniques," Reston Publishing Company, Inc., 1979 ("Gise")
Ex. 1011	Dillinger, "VLSI Engineering," Prentice Hall, 1988 ("Dillinger")
Ex. 1012	Nicollian, "Electrical Properties of the Si-SiO_2 Interface and its Influence on Device Performance and Stability," 14(5) J. Vac. Sci. Technol. 1112 Sept./Oct. 1977 ("Nicollian")

Further, Micron relies upon declaration testimony of its witness Michael L. Reed, Ph.D. (Ex. 1001: "Reed Decl.") originally submitted in this proceeding and declaration testimony of Robert M. Wallace, Ph.D. (Ex. 1003 pp. 452-59: "Wallace Decl.") previously submitted by the University during the prosecution of the '204 Patent.

1. Lisenker (Ex. 1004)

Lisenker discloses "a method for producing semiconductor devices in which hydrogen-containing bonds in silicon dioxide are replaced with deuterium containing bonds. Specifically Si-H bonds are replaced with Si-D

bonds and Si-OH bonds are replaced with Si-OD bonds." (P. 5, l. 36 – p. 6, l. 3.) Lisenker further discloses how the method may be carried out, stating:

> a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds in a silicon dioxide layer and on a silicon surface at an interface with the silicon dioxide layer. Typical silicon dioxide layers suitable for treatment according to the present invention include isolation oxides, gate oxides, and various other oxide layers commonly used with semiconductor devices. According to the invention, deuterium or a deuterium-containing material is directed onto the device by, for example, annealing in a deuterium containing atmosphere, and/or cleaning with a deuterium compound such as D_2O, D_2SO_4, and DCl. In general, any hydrogen containing material used in VLSI[6] fabrication can be replaced with corresponding deuterium containing material. (P. 4, ll. 20-34.)

Finally, Lisenker discloses the benefits of the method and how those benefits are obtained, stating:

> The stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms. The Si-D and Si-OD bonds thus formed provide completed silicon dangling bonds that are less likely to break when exposed to electrical stresses. Therefore, the deuterium containing devices of the present invention have improved stability, quality, and reliability. (P. 4, l. 35 – p. 5, l. 5.)

The University urges us not to consider the proposed grounds involving Lisenker because it was before the Office during prosecution. (Prelim. Resp. 8.) Under 35 U.S.C. § 325(d), "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to

[6] VLSI stands for "very large scale integration." (Ex. 1011, Dillinger 4.)

the Office." But, we are not required by statute to reject a petition based upon the fact that certain arguments or art were previously considered by the Office, and after reviewing the prior prosecution, we decline to do so in this case. The present record differs from the one before the Examiner. For example, we consider the Lisenker reference in view of the declaration testimony of Dr. Reed, which was not before the Examiner.

2. Ito (Ex. 1008)

Ito is entitled "Process For Producing A Semiconductor Device Having A Silicon Oxynitride Insulative Film." Ito states that "[t]he gate insulation film should have a thickness of from approximately 30 to 3000 angstroms[.]" (Col. 9, ll. 41-43.) Ito, at column 8, lines 38-42, further states:

> The insulative film, which is formed by a nitridation of the thermal oxidation of the silicon substrate, has such a structure that this oxidation film is gradually converted to silicon oxynitride from the surface to the interior of this film.

3. Nicollian (Ex. 1012)

Nicollian, at page 1121, states:

> The remaining problem is to maintain interface-trap and fixed-charge densities within specified limits during the life of the integrated circuit to insure stable operation. This stability is achieved by the use of coatings and encapsulants which isolate the device from its environment, and by operating the device at low temperatures so that changes in interface-trap and fixed-charge densities occur so slowly that device characteristics remain within specifications during device life.

4. Deal (Ex. 1009)

Deal is entitled "Complimentary Insulated Gate Field Effect Transistor Structure And Process For Fabricating The Structure." It discloses a field effect transistor with an interface between a semiconductive silicon layer and a gate oxide layer. (Col. 9, ll. 54-56.) Deal, at column 9, lines 33-53, states:

> The complementary field-effect transistor structure is then completed as shown in **FIG. 7** by applying conductive connectors and defining them to produce metal layer **50** which interconnects p-region **36**d and n-region **37**s and metal layers **51** and **52** which provide electrical contact with p-region **36**s and n-region **37**d, respectively. Interconnection of one source/drain region of the p-channel device and one source/drain region of the n-channel device produces a complementary field-effect circuit with the switching properties described above. . . . An anneal of the structure in a hydrogen-containing ambient in the temperature range of 350°-500° C. is carried out to minimize the fast interface state density, which also adversely affects threshold voltages and other device characteristics. Finally, scratch-protection layers and packaging is provided in accordance with established practices.

Deal does not disclose using deuterium for the above-described annealing.

5. Gise (Ex. 1010)

Gise is entitled "Semiconductor & Integrated Circuit Fabrication Techniques." Gise, at pages 130-31, states:

> Either during the alloy step or directly following it, the wafers are often exposed to a gas mixture containing hydrogen (or occasionally another gas). This step is usually called an "anneal" step. The anneal step is designed to optimize and stabilize device characteristics. Hydrogen is thought to combine with uncommitted atoms at or near the silicon-silicon

> dioxide interface, thus reducing their effect on device performance. Typical anneal temperatures are 400° – 500° C for times of 30 minutes to 60 minutes.

6. Mikawa (Ex. 1005)

Mikawa is entitled "Electron Spin Resonance Study of Interface States Induced by Electron Injection in Metal-Oxide-Semiconductor Devices." At page 2057, it states:

> It has often been proposed that hydrogen is involved in the electron trapping event in thermal oxides on silicon. In order to test this notion, we have subjected some sets of dry MOS oxides (described earlier) to 10% H_2/90% N_2 anneals and others to 10% D_2/90% N_2 anneals.

7. Reed Declaration (Ex. 1001)

Micron relies upon declaration testimony of Dr. Reed. Dr. Reed testifies that he has bachelor's, master's, and doctoral degrees in electrical engineering; has over twenty-five years of experience as a researcher and practitioner in electrical engineering; has industry experience as a process engineer focusing on integrated circuit processing and manufacturing of multi-project integrated circuit chips; and is currently a professor at the University of Virginia School of Engineering and Applied Science. (Reed Decl. ¶¶ 1-5.). We find Dr. Reed to be qualified to testify concerning the issues raised in the Micron Petition.

8. Wallace Declaration (Ex. 1003 pp. 452-59)

Micron relies upon declaration testimony of Dr. Wallace, submitted by the University during the prosecution, that "post metal hydrogen annealing had been in widespread use in the semiconductor industry for many years." (Wallace Decl. ¶ 15 (citing a 1995 article).)

E. The Asserted Grounds

Micron challenges the patentability of various subsets of claims 1-18 of the '204 Patent on numerous grounds as set forth on pages 3 and 4 of the Petition.

ANALYSIS

A. Claim Construction

We generally give claim terms their ordinary and customary meaning as would be understood by one of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc). In an inter partes review, "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b).

Pursuant to 37 C.F.R. § 42.104(b)(3), the Petition is to include a statement of how each challenged claim is to be construed. The Office Patent Trial Practice Guide ("Practice Guide"), however, states that "it may be sufficient for a party to provide a simple statement that the claim terms are to be given their broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure." 77 Fed. Reg. 48764 (Aug. 14, 2012). Micron has provided such a statement. (Pet. 5.)

The University asserts that the Petition should be denied because Micron has not provided the requisite claim construction. (Prelim. Resp. 16-17.) In so asserting, the University also relies on the Practice Guide, which further states "where a party believes that a specific term has meaning other than its plain meaning, the party should provide a statement identifying a proposed construction of the particular term and where the disclosure supports that meaning." 77 Fed. Reg. 48764. The University argues that

Micron is of the belief that several of the claims require a construction that is different than the plain meaning since, in the district court litigation involving the '204 Patent, Micron asserted that several claim terms required construction. (Prelim. Resp. 15 (citing Ex. 2004).) The record in this proceeding, however, lacks any constructions that may have been proposed by either party in the district court litigation.

We give each claim term its broadest reasonable interpretation as understood by one of ordinary skill in the art and consistent with the disclosure of the '204 Patent, as neither party has persuasively argued that any claim or term should be construed otherwise. For purposes of our Decision we find it useful to set forth, expressly, constructions for certain claim terms as follows.

1. Independent Claim 1

Each of independent claims 1, 6, 10, 13, and 14 includes a product-by-process limitation. For example, claim 1, as corrected by a December 20, 2005 Certificate of Correction (Ex. 1003 p. 569), states:

> 1. A semiconductor device comprising an n-channel field effect transistor . . . structurally characterized by the retention of deuterium at said interface *resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200° C.* so as to increase the resilience of the field effect transistor to hot electron effects during operation. (emphasis added).)

"[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself". *In re Thorpe*, 777 F.2d 695, 697 (Fed. Cir. 1985). Thus for patentability purposes, we look to the product claimed, not the process by which it is made. *See id.* ("If the product in a product-by-process claim is the same as

or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a difference process."); *Amgen Inc. v. F. Hoffman-LA Roche Ltd.*, 580 F.3d 1340, 1366 (Fed. Cir. 2009) ("It has long been the case that an old product is not patentable even if it is made by a new process.") (citing *General Elec. Co. v. Wabash Appliance Corp.*, 304 U.S. 364, 373 (1938)). Claim 1 requires the retention of deuterium at the interface. A reference teaching the retention of deuterium at the interface would meet this requirement even if formed by a process different than that which is claimed.

2. Independent Claims 6, 10, 13, and 14

Claim 6 recites a semiconductor device that, among other things, is:

> structurally characterized by post-fabrication heating of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200° C. to provide deuterium at and to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

Claim 10 recites a semiconductor device that, among other things, is:

> structurally characterized by a concentration of deuterium in said gate dielectric film at an interface with said semiconductive layer provided by heating the device, after formation of said source, drain and gate contacts, at a temperature of about 400° C. for about one hour in an atmosphere comprising about 10% deuterium and about 90% nitrogen, said transistor device susceptible to degradation associated with hot carrier stress, and said concentration of deuterium increasing the resilience of the field effect transistor to channel hot carrier stress.

Claim 13 recites a semiconductor device that, among other things, is:

> structurally characterized ... by the presence of deuterium at said interface resulting from post-fabrication passivation of said interface in a heated, deuterium gas-enriched atmosphere at a temperature above about 200° C. so as to increase the resilience of the field effect transistor to hot electron effects, said post-fabrication passivation being conducted sufficiently to provide to said transistor a practical lifetime at least about ten times that provided by a corresponding passivation with hydrogen, wherein practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

Claim 14 recites a semiconductor device that, among other things, is:

> structurally characterized ... by annealing of the device after formation of at least said gate contact, in a deuterium gas-enriched atmosphere at a temperature above about 200° C. to provide deuterium at said interface between said gate insulating layer and said channel to passivate said interface so as to increase the resilience of the field effect transistor to hot electron effects.

We construe each of the above-quoted limitations of claims 6, 10, 13, and 14 to require deuterium at the interface. A reference teaching deuterium at the interface would meet this requirement even if formed by a process different than that which is claimed *See Thorpe*, 777 F.2d at 697; *Amgen*, 580 F.3d at 1366.

3. Independent Claim 15

Independent claim 15 requires "a concentration of deuterium introduced into and remaining in said interposed gate insulator film[.]"[7] Claim 15 does not require post-metal deuterium annealing.

[7] Claim 15 was corrected by the December 20, 2005 Certificate of Correction (Ex. 1003 p. 569).

4. Dependent Claim 9

Claim 9 is dependent on claim 6 and additionally recites "deuterium atoms from said post-fabrication passivation covalently bonded at said interface." This is a product-by-process limitation, which we construe to require deuterium atoms covalently bonded at the interface. A reference teaching deuterium atoms covalently bonded at the interface would meet this requirement even if the result of a process different than that which is claimed. *See Thorpe*, 777 F.2d at 697; *Amgen*, 580 F.3d at 1366.

B. Claims 6-8 As Obvious Over Kwong

As set forth above, we construe claim 6 to require deuterium at the interface, and claims 7 and 8 depend from claim 6. Kwong does not disclose deuterium at the interface or the use of deuterium at all.

Accordingly, based on the record before us, there is a not reasonable likelihood that Micron will prevail on its assertion that claims 6-8 would have been obvious over Kwong.

C. Claims 6-8 As Obvious Over Ito

Ito, like Kwong, does not disclose deuterium at the interface or the use of deuterium at all.

Accordingly, based on the record before us, there is a not reasonable likelihood that Micron will prevail on its assertion that claims 6-8 would have been obvious over Ito.

D. Claims 1, 2, 4, and 5 As Anticipated By Lisenker

Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros., Inc. v. Union Oil Co. of Cal.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

1. Claim 1

Claim 1 requires "an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer[.]"

Lisenker expressly discloses a field effect transistor. (*See, e.g.*, p. 1, l. 16 (disclosing a "MOSFET")[8]; p. 11, l. 6. (disclosing "MOS transistors")[9].) We credit the testimony of Dr. Reed that the Lisenker field effect transistor is of the n-channel type because "a disclosure referencing MOSFETs would be applicable to N-channel MOSFETs unless explicitly directed otherwise." (Reed Decl. ¶ 10.) We also credit his testimony that "Lisenker's reference to MOSFET devices necessarily includes N-channel devices. For example, Lisenker's discussion of hot electrons (the N-type carrier) produced in the channel region indicates that the channel is N-type." (Reed Decl. ¶ 34 (citing Lisenker col. 4, ll. 2-10).) The University has not argued that the Lisenker MOSFET is not an n-channel field effect transistor.

Lisenker does not expressly disclose all of the sub-structures of the field effect transistor that are recited in claim 1. Micron argues that these structures are inherent to a MOSFET, based primarily on the following testimony of Dr. Reed:

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[8] A MOSFET is a metal oxide semiconductor *field effect transistor.* ('204 Patent col. 1, ll. 44-45 (emphasis added).)

[9] Dr. Reed testified that "in the semiconductor industry, the term 'MOS transistor' is understood to mean MOS field effect transistor." (Reed Decl. ¶ 34.)

> All MOSFETs have a gate insulating layer interposed between a semiconductor substrate, typically silicon, and a gate electrode. In the semiconductor layer, a channel extends between a drain and source. Electrical connections to the gate, source, and drain are made through ohmic contacts. Voltages are applied to these contacts in order to regulate the conductivity of the channel and the current flowing between the source and drain. These elements set forth above are necessarily present in a MOSFET such that the disclosure or discussion of a MOSFET in a reference would include the disclosure of each of its attendant elements. (Reed Decl. ¶ 9; *see also* Reed Decl. ¶ 34.)

Based on the present record, including the testimony of Dr. Reed quoted above and which we credit, we find that Lisenker discloses the limitation of "an n-channel field effect transistor including a drain formed in a semiconductive layer, a source formed in said semiconductive layer, a channel extending between the drain and the source, a gate insulating layer over said channel, an interface between a semiconductive silicon layer and a gate insulating layer, and conductive contacts to said drain, source and on said gate insulating layer" as required by claim 1. The University does not dispute that Lisenker discloses the limitation.

Claim 1 additionally requires the retention of deuterium at said interface so as to increase the resilience of the field effect transistor to hot electron effects during operation. Lisenker expressly discloses the retention of deuterium at the interface:

> The regions where the deuterated bonds provide the greatest benefit in terms of device performance is at the interface of silicon-silicon dioxide layers. Thus, the semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially

> greater than ratio of naturally occurring deuterium to hydrogen. (P. 10, ll. 29-35.)

The claimed "increase in resilience of the field effect transistor to hot electron effects during operation" is an inherent result of the Si-OD and Si-D bonds at the interface, and Lisenker expressly recognizes this result. (P. 5, ll. 4-5 ("[D]euterium containing devices of the present invention have improved stability, quality, and reliability."))

Based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 1 is anticipated by Lisenker.

2. Claims 2, 4, and 5

Claims 2, 4, and 5 are each dependent on claim 1. Claim 2 additionally requires that the "gate insulating layer comprises silicon dioxide." Claim 4 additionally requires that the "gate insulating layer comprises an oxide of silicon." Claim 5 additionally requires that the "gate insulating layer comprises silicon dioxide or silicon oxy nitride."

Lisenker discloses all of these additional limitations, as it discloses the use of silicon as the semiconductive layer and silicon dioxide in the gate insulator. (P. 4, ll. 20-27.)

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claims 2, 4, and 5 are anticipated by Lisenker.

E. Claims 1, 2, 4-7, 9-16, and 18 As Obvious Over Lisenker

1. Claims 1, 2, 4, and 5

For reasons similar to those discussed above, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1, 2, 4, and 5 would have been obvious over Lisenker. Further, we credit Dr. Reed's

testimony that "post-metallization annealing in hydrogen was a standard process step in integrated circuit fabrication to passivate defects created previously in the fabrication process" such that we conclude that it would have been apparent to one skilled in the art to perform Lisenker's deuterium annealing process after the metallization steps have been performed. (Reed Decl. ¶¶ 35-36).

2. Claims 6, 10, 13, 14, and 15

Each of independent claims 6, 10, 13, 14, and 15 is similar to claim 1 and additionally requires a gate insulating/dielectric layer/film "having a thickness not exceeding about 55 Angstroms[.]" We find that Lisenker, as discussed above and below, teaches the subject matter of these claims except for the thickness limitation.

The Supreme Court has held that the obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). In that regard, we credit the testimony of Micron's witness, Dr. Reed that, at the time of filing the '204 Patent, it would have been apparent to reduce the thickness of the gate insulating film of Lisenker to about 55 Angstroms or less consistent with the general decades-long trend of device miniaturization in the semiconductor industry. (Reed Decl. ¶ 38.)

We also credit Dr. Reed's testimony that, at the time of filing the '204 Patent, others already had made gate insulating films having thicknesses of about 55 Angstroms or less. (Reed Decl. ¶ 39 (citing Kwong col. 1, ll. 40-45); Reed Decl. ¶ 43 (citing Ito col. 9, ll. 39-62).) The combination of

familiar elements according to known methods to achieve predictable results, such as reducing the thickness of the gate insulating film of Lisenker to 55 Angstroms or less, is likely to be obvious. *See KSR*, 550 U.S. at 401.

Accordingly, based on the present record, which lacks sufficient evidence of criticality of the thickness limitation, there is a reasonable likelihood that Micron will prevail on its assertion that claims 6, 10, 13, 14, and 15 would have been obvious over Lisenker to a person of ordinary skill in the art under 35 U.S.C. § 103(a).

We have considered the University's preliminary arguments but we do not find them persuasive as discussed below.

The University does not rely on the gate insulator thickness limitation as distinguishing its claimed inventions over the prior art. Rather, the University argues that "[t]he independent claims generally have two distinctive limitations: (1) the deuterium anneal is performed post-fabrication, or after the formation of the metal contacts; and (2) the post-fabrication anneal results in a device where the deuterium is retained at the interface of the semiconductive layer and gate insulator." (Prelim. Resp. 2.)

This argument is based on the premise that the '204 Patent claims require post-metal (i.e., post-fabrication) deuterium annealing. As construed above, they do not.

The University next argues that Lisenker teaches away from the claimed invention "because the deuterium added during a pre-fabrication anneal would migrate away from the interface due to subsequent thermal processing required to fabricate the metal layers." (Prelim. Resp. 7.) We do not find this argument persuasive for multiple reasons. First, Lisenker is not limited to substituting deuterium for hydrogen only during pre-metal

annealing. Rather, Lisenker teaches that it "can be implemented throughout the VLSI fabrication procedure" including during the "various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps" of a typical fabrication procedure. (P. 8, ll. 29-35.) Second, the University's teaching away argument is directly at odds with the Lisenker disclosure, which expressly states that deuterium will be present at the interface. (P. 10, ll. 29-35.)

The University also argues that post-metal deuterium annealing (as opposed to pre-metal deuterium annealing) yielded results that were unexpected at the time of the filing of the '204 Patent. (Prelim. Resp. 7-8.) This argument, however, is not commensurate with the scope of the claims, which do not require post-metal deuterium annealing.

Based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 6 would have been obvious over Lisenker to a person of ordinary skill in the art.

3. Claims 7, 11, 12, and 16

Claim 7 is dependent on claim 6 and additionally requires that the "gate insulating layer comprises silicon dioxide."

Claim 11 is dependent on claim 10 and additionally requires that the "the semiconductive layer comprises silicon, and the gate dielectric film includes a silicon compound."

Claim 12 is dependent on claim 11 and additionally requires that the "silicon compound comprises an oxygen or a nitrogen containing silicon compound."

Claim 16 is dependent on claim 15 and additionally requires that the "gate insulator comprises an oxide of silicon."

Lisenker discloses all of these additional limitations, as it discloses the use of silicon as the semiconductive layer and silicon dioxide in the gate insulator. (P. 4, ll. 20-27.)

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 7, 11, 12, and 16 would have been obvious over Lisenker to a person of ordinary skill in the art.

4. Claim 9

Claim 9 is dependent on claim 6 and additionally recites "deuterium atoms from said post-fabrication passivation covalently bonded at said interface." We have construed this product-by-process limitation to require deuterium atoms covalently bonded at the interface, not post-fabrication passivation.

Lisenker discloses deuterium atoms in covalent bonds. (P. 5, ll. 15-24 ("Devices of this invention will preferably have substantial numbers of Si-H and/or Si-OH bonds replaced with Si-D and/or Si-OD bonds.").) Lisenker further illustrates such bonds at the interface in Figure 1, reproduced below.

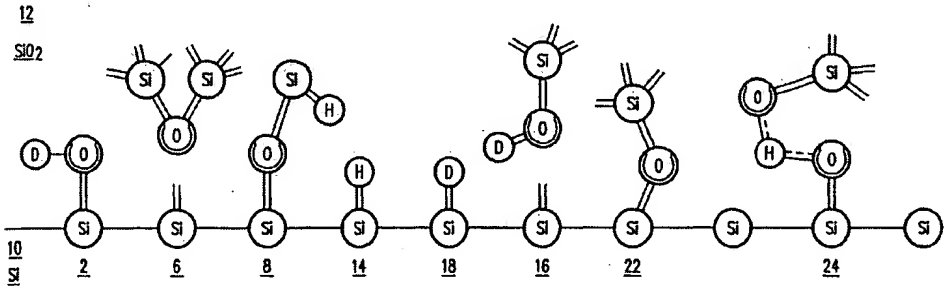

FIG. 1

Figure 1 illustrates a silicon-silicon dioxide interface

As is evident from Figure 1, there are deuterium atoms in covalent bonds at positions 2 and 18 of the illustrated interface.

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 9 would have been obvious over Lisenker to a person of ordinary skill in the art.

5. Claim 18

Claim 18 is dependent on claim 15 and additionally requires that the "the field effect transistor comprises an n-channel device subject in operation to hot electron stress." As set forth above, based on Dr. Reed's testimony, we find that Lisenker discloses the limitation of an n-channel field effect transistor. We also find that, if Lisenker does not actually disclose a field effect transistor of the N-channel variety, it nevertheless suggests it. In that regard, we credit Dr. Reed's testimony that "Lisenker's discussion of hot electrons (the N-type carrier) produced in the channel region indicates that the channel is N-type." (Reed Decl. ¶ 34 (citing Lisenker p. 4, ll. 2-10).) The University does not dispute that Lisenker discloses the limitation.

Accordingly, based on the present record, there is a reasonable likelihood that Micron will prevail on its assertion that claim 18 would have been obvious over Lisenker to a person of ordinary skill in the art.

F. Claims 1, 2, 4-7, 9-16, and 18 As Obvious Over Lisenker and Gise

Micron additionally relies on Gise as allegedly teaching a post-metal annealing (in hydrogen) for about an hour. Gise does teach this. (Gise pp. 130-31.) Further, we credit the testimony of Dr. Reed that "it would have been apparent to perform Lisenker's annealing process after the

metallization steps have been performed" in light of Gise's teaching. (Reed. Decl. ¶ 36.)

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1, 2, 4-7, 9-16, and 18 would have been obvious over Lisenker in view of Gise to a person of ordinary skill in the art.

G. Claim 3 As Obvious Over Lisenker, Gise, and Nicollian

Claim 3 is dependent on claim 1 and additionally requires that the semiconductor device "is encapsulated." Nicollian discloses "the use of coatings and encapsulants" to isolate a semiconductor device from its environment to promote stable operation of it. (Nicollian p. 1121.) We credit the testimony of Dr. Reed that encapsulation "has long been incorporated into integrated circuit manufacturing" and that "[a]t the time of the priority date of the '204 patent, it would have been apparent to include an encapsulation step as taught by Nicollian in the device of Lisenker in order to prevent physical damage and corrosion to the semiconductor device." (Reed Decl. ¶¶ 45-46.)

Accordingly, based on the record before us, there is a reasonable likelihood that Micron will prevail on its assertion that claim 3 would have been obvious over Lisenker, Gise and Nicollian.

H. Claims 6-18 As Obvious Over Lisenker, Gise, and Ito

Micron relies on Ito for teaching two things: (1) a gate insulator having a thickness not exceeding about 55 Angstroms (as required by all of claims 6-18); and (2) a gate insulator comprising silicon oxynitride (as required by claims 8 and 17).

We already have determined above that there is a reasonable likelihood that Micron will prevail on its assertion that claims 6, 7, 9-16, and 18 would have been obvious over Lisenker alone as well as over Lisenker in view of Gise. In doing so, however, we did not find an express teaching within Lisenker or Gise of the thickness limitation of about 55 Angstroms or less.

Ito provides an express teaching of gate insulative layers as thin as approximately 30 Angstroms. (*See* col. 9, ll. 41-43). Ito also teaches gate insulative layers that comprise silicon oxynitride, at column 8, lines 38-42, stating:

> The insulative film, which is formed by a nitridation of the thermal oxidation of the silicon substrate, has such a structure that this oxidation film is gradually converted to silicon oxynitride from the surface to the interior of this film.

We credit the testimony of Dr. Reed that, at the time of the priority date of the '204 patent, it would have been apparent to substitute Ito's thin insulating layer comprising oxynitride for the silicon dioxide layer disclosed by Lisenker because miniaturization of semiconductor elements was a common endeavor among those in the semiconductor industry and because silicon oxynitride was known to improve the resilience of MOSFETs to hot carrier effects. (Reed Decl. ¶ 44.)

Based on the present record, including reasons already discussed above with respect to the teachings of Lisenker and Gise, there is a reasonable likelihood that Micron will prevail on its assertion that claims 6-18 would have been obvious over Lisenker, Gise and Ito to a person of ordinary skill in the art.

I. Claim 10 As Obvious Over Lisenker, Gise, Ito, and Mikawa

With respect to claim 10, Micron relies on Mikawa as teaching passivation using a forming gas comprising about 10% hydrogen and 90% nitrogen. (Pet. 59.)

As we already have determined that there is a reasonable likelihood that Micron will prevail on its assertion that claim 10 would have been obvious over Lisenker, Gise, and Ito, we also conclude that there is a reasonable likelihood that Micron will prevail on its assertion that claim 10 would have been obvious over Lisenker, Gise, and Ito in further view of Mikawa.

J. Claims 1-5 As Obvious Over Deal and Lisenker

Micron asserts that Deal teaches the subject matter of these claims except for the retention of deuterium at the interface. (Pet. 28-29.) We agree and note that the University has not, in its Preliminary Response, disputed the asserted teachings of Deal.

Micron next asserts that it would have been obvious for a person of ordinary skill in the art at the time of the invention of the '204 Patent to modify Deal to employ deuterium instead of hydrogen as taught by Lisenker to increase the resiliency of the field effect transistor to hot electron effects. (Pet. 28-29.) We credit the testimony of Dr. Reed and in particular that portion set forth at paragraph 49 of his testimony, which states:

> At the time of the priority date of the '204 patent, the benefits of substituting deuterium for hydrogen were known. As I have discussed previously, Lisenker teaches the substitution of deuterium for hydrogen and states that such a substitution results in "bonds that are less likely to break when exposed to electrical stresses," which improves device "stability, quality, and reliability." It would have been apparent to incorporate the

> teachings of Lisenker with the '380 patent [i.e., Deal] because both references are directed to improving the quality of the Si/SiO2 interface, which has a direct impact on the device quality. Lisenker suggests that "any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material," which would include the '380 patent's post-metallization anneal.

Based on the present record, there is a reasonable likelihood that Micron will prevail on its assertion that claims 1-5 would have been obvious over Deal and Lisenker to a person of ordinary skill in the art.

K. Claims 6-18 As Obvious Over Deal, Lisenker, and Ito

Here, Micron again relies on Ito for teaching a gate insulator having a thickness not exceeding about 55 Angstroms (as required by claims 6-18), which gate insulator comprises silicon oxynitride (as required by claims 8 and 17).

As set forth above, we credit the testimony of Dr. Reed that, at the time of the priority date of the '204 patent, it would have been apparent to substitute Ito's thin insulating layer comprising oxynitride for the silicon dioxide layer disclosed by Lisenker because miniaturization of semiconductor elements was a common endeavor among those in the semiconductor industry and/or silicon oxynitride was known to improve the resilience of MOSFETs to hot carrier effects. (Reed Decl. ¶ 44.)

Accordingly, based on the present record, including reasons already discussed above with respect to the teachings of Deal and Lisenker as applied to claims 1-5, there is a reasonable likelihood that Micron will prevail on its assertion that claims 6-18 would have been obvious over Deal, Lisenker, and Ito to a person of ordinary skill in the art.

L. Other Asserted Grounds

The remaining asserted grounds of the Petition (*see* pp. 3-4) are unnecessary as cumulative in light of the determination that there is a reasonable likelihood that claims 1-18 are unpatentable as set forth above.

SUMMARY

Petitioner, Micron, has demonstrated that there is a reasonable likelihood of prevailing on its challenge to the patentability of all claims of the '204 Patent.

The Petition is granted as to the following grounds:

I. Claims 1, 2, 4, and 5 as anticipated by Lisenker;

II. Claims 1, 2, 4-7, 9-16, and 18 as obvious over Lisenker;

III. Claims 1, 2, 4-7, 9-16, and 18 as obvious over Lisenker and Gise;

IV. Claim 3 as obvious over Lisenker, Gise, and Nicollian;

V. Claims 6-18 as obvious over Lisenker, Gise, and Ito;

VI. Claim 10 as obvious over Lisenker, Gise, Ito, and Mikawa.

VII. Claims 1-5 as obvious over Deal and Lisenker; and

VIII. Claims 6-18 as obvious over Deal, Lisenker, and Ito.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that the Petition is granted as to claims 1-18 of the '204 Patent on the grounds identified as I – VIII above;

FURTHER ORDERED that the Petition is denied on all grounds not identified as I – VIII above;

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(a), inter partes review of the '204 Patent is hereby instituted commencing on the

entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; and

FURTHER ORDERED that an initial conference call with the Board is scheduled for 2:00 PM ET on April 9, 2013. The parties are directed to the Office Trial Practice Guide, 77 Fed. Reg. 48756, 48765-66 (Aug. 14, 2012) for guidance in preparing for the initial conference call, and should come prepared to discuss any proposed changes to the Scheduling Order entered herewith and any motions the parties anticipate filing during the trial.

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